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O.I.P.E. SCANNED <i>ggc</i> Q.A. <i>AA</i>	PATENT DATE
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APPLICANTS	APPLICATION NO.	CONT/PRIOR	CLASS	SUBCLASS	ART UNIT	EXAMINER
	09/785604		370 713	500	2661 <del>5000</del>	LIE Du

2116

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TITLE

Method and apparatus for distributing a self-synchronized clock to nodes on a chip

PTO-2040  
12/89

[illegible]

<input type="checkbox"/> <b>TERMINAL DISCLAIMER</b>	<b>DRAWINGS</b>		<b>CLAIMS ALLOWED</b>					
	<b>Sheets Drwg.</b>	<b>Figs. Drwg.</b>	<b>Print Fig.</b>	<b>Total Claims</b>	<b>Print Claim for O.G.</b>			
<input type="checkbox"/> The term of this patent subsequent to _____ (date) has been disclaimed.	_____ (Assistant Examiner)		<b>NOTICE OF ALLOWANCE MAILED</b> _____ (Date)					
<input type="checkbox"/> The term of this patent shall not extend beyond the expiration date of U.S. Patent No. _____ _____ _____	_____ (Primary Examiner)		<b>ISSUE FEE</b> <table border="1"> <tr> <td><b>Amount Due</b></td> <td><b>Date Paid</b></td> </tr> <tr> <td> </td> <td> </td> </tr> </table>		<b>Amount Due</b>	<b>Date Paid</b>		
<b>Amount Due</b>	<b>Date Paid</b>							
<input type="checkbox"/> The term _____ months of this patent have been disclaimed.	_____ (Legal Instruments Examiner)		<b>ISSUE BATCH NUMBER</b> _____					
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(FACE)